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SMART POWER FACTOR CONTROL STRATEGIES FOR ADVANCED INTERIOR PERMANENT MAGNET (IPM) MOTORS

Muhammad Arif[1], Khawaja Tahir Mehmood[*2], Muhammad Aamir Shafi[3]

[1, *2]*Department of Electrical Engineering, Bahauddin Zakariya University, Multan, 60000, Pakistan*
[3]*Instituto de diseño y Fabricación (IDF)-Universitat Politécnica de València (UPV), Spain*

[*2]ktahir@bzu.edu.pk

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Corresponding Author: *
Khawaja Tahir Mehmood

Abstract
New AC motor-drive systems require high power-factor operation and strong speed control to be efficient, minimize line losses and enhance the quality of power. Traditional rectifier-inverter front-ends have low power factor and higher harmonic distortion particularly under dynamic load operation leading to increased current stress and unstable motor operation. In order to overcome these shortcomings, this paper suggests a combined power-factor enhancement and speed-control approach to an interior permanent-magnet (IPM) motor drive. This paper presents a novel method of Power factor improvement, which consists of an ac power source, a diode rectifier bridge, dc-link capacitor, PWM driven inverter and interior permanent magnet motor. The inverter plays two critical roles: (1) It enhances the quality of input supply current to be closer to the ideal sine waveform in order to have Power factor of unity and (2) varying of motor speed in compensating increase in current resulted due to sudden decrease in the voltage observed during overloading conditions. In this approach three phase current of inverter (I_a, I_b, I_c) and rotor angle(α) of IPM motor are employed to transform the three-phase model into d-q axis (I_d, I_q). The actual motor speed (Wm) is compared with the reference speed (W_r) by PID speed controller, whose output is demanded current (I_{dem}). The model d-q currents (I_d, I_q) are compared with sought current (I_{dem}) through PID current controller to obtain desired current (I_d, Iq). The reference d-q currents are then converted back into three phases (I_a, I_b, I_c). These are compared with a triangular carrier wave to produce PWM signals which serve as gating pulses for the inverter. The inverter commences using 120∘ PWM pattern and then the inversely generated PWM signals are applied to IGBTs. This method provides PF improvement and reduces current ripple and harmonics together.

INTRODUCTION

The widespread application of electric apparatuses in domestic and industrial fields develops fast, great convenience, high efficiency is achieved at the same time accompanying enormous problems power system facing[1-3]. The voltage regulation is poor, reactive power demand and harmonics distortion are higher, load is shed off, PF is low which affecting the system reliability due to the overload condition. For a stable and reliable power system operation, Power Quality Improvement (PQI) is now an essential requirement. It is very common to use variable speed drives in power factor correction (PFC) circuits, so the harmonics are suppressed, and transmission efficiency will increase, a near-unity power factor being reached. Heavy copper losses, poor voltage regulation and reduced capacity are the results of low

power factor conditions, and the economics of a power system is directly affected by it. Penalty applied by WAPDA to industrial consumers for running at low power factor is given by Equation 1:

Penalty=Difference×2×MDI (kWh)×400 Rs/kWh (1)

Where, Difference = (actual power factor - 0.9) And MDI: Maximum Demand Indicator: This is the amount of energy consumption in kwh by a consumer during any given period. The 400 Rs/kWh is the tariff rate for industrial user. For instance, for power factor of 0.85 and MDI of 567 kWh, the penalty is (0.90−0.85) ×2×567×400=22,680 Rs. These charges emphasize the cost consequences of low power factor operation. Nevertheless, this can be easily overcome by using power factor correction (PFC) methods which are well documented in the literature. Conventional PFC schemes require reactors, electrolytic capacitors and supplementary switching components which are expensive and space-consuming [4-6]. The resulting devices also have higher power losses, most of which are absorbed by the reactor and with the electrolytic capacitor often being a lifetime limiting component of the converter. In addition, they need bulky noise filters resulting in high-cost antenna system. Significantly these techniques mainly control the output voltage waveform and not the output current waveform, leaving harmonics and ripple content at distorted levels that do not provide satisfactory performance. Accordingly, voltage and current waveforms are not smooth, and the effect of improving the power factor is also restricted [7-10]. Unlike [11], the proposed strategy in literature does not employ huge energy storages (reactors), electrolytic capacitors and noise filters. But it adopts a sophisticated control law to obtain (Id*, Iq*), which needs a lot of other control equipment and makes the system complex and expensive [12-15]. Though the power factor enhancement is better in this technique as compared to previous one, the current waveform and voltage waveform are still with significant ripples. Instead, the technique developed in this work is more cost-effective and easier to realize, leading to unity power factor operation. It further smoothens the current and voltage waveforms (compensation for conventional methods but not achievable at previously proposed ones) [16-18]. Conventional PFC methods use reactors, electrolytic capacitors and extra sets of switches which are bulky, costly and inefficient. Reactors will cause a large power loss while the electrolytic capacitor usually is one of the factors deciding its lifetime. These methods are also based on huge noise filters, which leads to complex restoration and expensive price. In addition, existing PFC control methods mainly control the output voltage waveform not the output current waveform efficiently; therefore, the levels of harmonics and ripples are maintained at a level that rather degrades system performance [19-21]. This results in non-sinusoidal current and voltage waveforms, so that the power factor improvement is not satisfactory. It is seen that the method described in literature does away with bulky reactors, electrolytic capacitors and large noise filters [22]. But it requires complicated control method to get (Id^*, Iq^*) and multi-control devices are used, thus incurring high cost and the difficulty to achieve. This approach provides effective power factor correction as compared to the conventional methods, however the current and voltage waveforms developed are ripple [23-24]. A PMSM is chosen as the IPM motor in this work. In PMSM, the rotor contains permanent magnets mounted on its surface that provide additional magnetic field to produce torque. Further, no air gap leakage flux allows for constant speed regardless of load change or supply voltage fluctuation. These features make PMSM a preferred choice for CPS drives application. It is well known that synchronous motors are connected in parallel with the lines to cause leading currents and thus increase the power factor [25-27]. This is the reason why PMSM presents in proposed PFC circuit. It can be seen that the Id and Iq values above have been acquired directly from the PMSM motor, but in such case several voltage and current limiters must be used. So, in the proposed scheme these values are produced by a PWM-controlled inverter**.** Another key factor here is to rapidly convert 3-axis mode or 2-axis mode into one another, and vice versa, allowing for performance of desired goals [28-30]. This approach is utilized to command the turn-on of IGBTs in such a way that they are able to get a unity power factor. The relation between the 3-axis (Ia, Ib, Ic) and d-q model is given by Equation (2-4):

$$\begin{bmatrix} Iqsat \\ Idsat \end{bmatrix} = \begin{bmatrix} cos\theta & cos(\theta - 120\circ) & cos(\theta + 120\circ) \\ sin\theta & sin(\theta - 120\circ) & sin(\theta + 120\circ) \end{bmatrix} \begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} \quad (2)$$

$$I_q = 2I_a - I_b - I_c \quad (3)$$

The formula for I_{dsat} is a conversion that accounts for the three-phase currents to the d-axis component:

$$I_{dsat} = -\frac{1}{\sqrt{3}} I_b + \frac{1}{\sqrt{3}} I_c \quad (4)$$

Likewise, the inverse conversion matrix is given in Equation (5)

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\theta - 120° & \sin\theta - 120° & 1 \\ \cos\theta + 120° & \sin\theta + 120° & 1 \end{bmatrix} \begin{bmatrix} Iqsat \\ Idsat \\ Iosat \end{bmatrix} \quad (5)$$

It is possible to transform the stationary d-q model into the spinning d-q model. The following are the Equations (6-7):

$$I_q = Iqsat \cos\theta - Idsat \sin\theta \quad (6)$$

$$I_d = Iqsat \sin\theta + Idsat \cos\theta \quad (7)$$

In the proposed approach, rotor angle (θ) of PMSM is used in sine and cosine computations for the said transformations. A pulse delay block is placed so that the inversely generated PWM modulation signals do not simultaneously turn on the IGBTs of two inverter legs, causing a shot circuit.

1.1. Work Contribution

A novel power factor correction approach which is more cost-effective, less complex to implement and capable of realizing zero phase operation with supply mains Congestion This article suggests a novel method of improving the power factor. Unlike conventional and reported methods, the proposed method achieves smoother current and voltage waveforms with low harmonics and ripples. This has made it an economical answer for modern industrial and home applications where energy efficiency and power quality are crucial requirements.

1. **Integrated Control Framework:** The algorithm integrates inverter current feedback (Ia, Ib, Ic), and rotor angle (α) transforms to d–q reference frame for accurate control using cascaded PID speed and current controllers.
2. **Dual-Stage PWM Operation:** This paper uses special two-stage modulation method—inverse PWM modulation control after 120∘ phase reduced ripple current waveform/input harmonics wave.
3. **Overload Protection and Stability:** The proposed scheme can efficiently control motor speed during the occurrence of voltage sags and overload cases at which current raising is prevented and stable operation guaranteed.
4. **Suitability for Next-Generation Applications:** This approach offers a strong and energy-efficient solution for contemporary IPM motor applications, improving grid compatibility as well as drive reliability.

1.1.1 Research Highlights

1. For IPM motor drives, a novel power factor adjustment toward unity is suggested in this study.
2. For precise dynamic control, the d-q transform is applied with cascaded PID speed and current controllers.
3. A two-stage PWM control (120° PWM in normal and inverse modes) reduces harmonics and ripples in current.
4. Under typical circumstances, the suggested approach can preserve driving stability while lowering voltage dips and significant current surges under over-load.
5. It has improved grid compatibility, an inverter, and a high-performance, lightweight IPM motor solution for the future.

1.2. Research objectives

1. Primary Goal Focused: To design and verify power factor correction technique for IPM motor drives to k will be operation with near unity power factor and good input current quality.
2. Comprehensive Technical Objective: To develop an effective control approach for IPM machine drives that not only enhances power factor and reduces current harmonics/ripples but also

ensures stable motor system operation under variable load and voltage.

3. Control-Oriented Objective: To achieve an efficient d–q model-based control scheme with PID controllers and PWM techniques to improve power factor correction and dynamic speed response for IPM motor drives.

4. Application-Oriented Objective: To offer a reliable power factor control for the new-IPM-motorization generation that improves efficiency and extends life of the supply network and of overall drive.

The literature research and a comparison of the proposed framework with traditional fault management strategies are covered in Section 2. Section 3 discusses the methodology to achieve the intended goal. The simulation findings and the conclusion are discussed in the final section.

2 Literature Review

(a)The traditional PFC used on Motor Drives:

Classical diode-bridge based front ends with a DC-link and VSI are small components that are strong but have low power factor and high input current THD when loaded dynamically. What is becoming a popular fix, which draws near-sinusoidal line current and harmonizes the DC connection even with mains variations, is adding a boost PFC stage at the cost of more parts and losses [31-33].

(b) Active Rectifier Topologies Active rectifier topologies:

At the cost of increased control complexity, PWM rectifiers, and the Vienna rectifier family offer unity power factor with low THD and bidirectional energy flow (in the case of PWM AFE), but at the cost of increased control complexity [34-36]. Experiments indicate Vienna rectifiers achieve less than 5% THD and near-unity PF in power systems operating with high power and can also be used to improve the quality of mains current in AC drive systems [37-39].

(c) Inverter Motors Inverter-motor-centric PFI (Removal of the Front-End PFC):

Another stream incorporates PFI within the motor drive taking advantage of the inverter and the electromechanics of the machine, and use a small film capacitor rather than a large electrolytic. Leading the way with IPM operation demonstrated that it was possible to shape inverter currents (and hence source current) to only a small fraction short of unity PF without any inductive/capacitive PFC equipment; recent studies have examined small-cap DC links to PMSM/IPMSM with high PF and reasonable ripple[40-43].

(d) Synchronous dq Frame Control:

In the Synchronous dq Frame, the control is decentralized and functions using a packet-based format, designed to operate without centralizing control to facilitate scalability, the control is not centralized and is based on a packet-based format, which is intended to be used without a control centralization to support scalability[44-46]. In IPMSM motors, field-oriented control (FOC) through Clarke Park transforms splits stator current into torque-generating i distortion and flux-linked $i$dt channels, which allow speed and current to be directly controlled with PID (or high-technology) loops. Recent surveys and tutorials verify that FOC is the default standard of high-performance IPM drives; new versions modify the coordinate frame or provide parameter variation resilience.

(e) Dynamic Disturbances:

Adjustable-speed drives experience voltage sags and current surges that run-up owing to overloads and deteriorate PF and stability [47-50]. Control-oriented works provide the description of the ride-through strategies (feed-forward DC-link compensation, torque-control adjustments, or speed-loop coordination) to ensure the currents are kept within the limits and assure the torque. These publications drive combined designs in which the inverter controls speed besides modeling input current as opposed to using additional hardware PFC.

(f) Context of Compliance & Power-Quality:

The current-distortion and harmonic limits (current-distortion and harmonic) of a current-distortion-conforming PCC and equipment to 16 A/phase or larger are defined by modern standards (IEEE 519 (2014/2022)) and limits (IEC 61000-3-2/-3-12) [51-52]. The designs which reduce the front-end harmonics at the expense of unity PF directly overcome these regulatory limitations.

2.1 Gap & Rationale

While boost-PFC and Vienna/PWM-AFE rectifiers achieve excellent PF/THD, they add cost, volume, switching loss, and control overhead. Conversely, drive-embedded PFI using the VSI + IPM machine reduces hardware stages and electrolytic dependence, yet literature is thinner on co-optimizing input current quality and speed regulation under sags/overloads with 120° carrier-based PWM and PID cascades in dq. This gap motivates an integrated approach that transforms $(i_a, i_b, i_c, \alpha) \rightarrow (i_d, i_q)$, commands $i_{d,\text{ref}}$from the speed loop, tracks i_d, i_qvia current loops, and inverse-transforms to generate PWM gating—explicitly targeting near-unity PF, lower THD/ripple, and robust speed control under grid disturbances.

3. Research Methodology

The proposed power factor derating system includes an AC power supply, a diode bridge rectifier, a DC side capacitor, a pulse width modulated (PWM)-inverter and an interior permanent magnet motor. The inverter has two important jobs: (1) Enhancing the pureness of input supply current much closer to purely sinusoidal waveform and meanwhile, with unity power factor is obtained. (2) Controlling the speed of an electrical motor in order to prevent excessive current increase during sudden voltage drops due to overload. Figure 1 depicts the working of a proposed model. Block Diagram The block diagram of the system can be divided into two parts: 1) Main system 2) PFC circuit.

3.1 Main Circuit Description

The system is driven by three-phase AC voltage, with ammeters and voltmeters for the measurement of current and voltage. The measurements obtained provide the data to check variations of power factor at various loading statuses. There is also connected a three-phase circuit breaker to isolate said PFC at the same time a step input signal.

3.2 PFC Circuit Description

The system under consideration includes a single-phase AC source, a diode rectifier bridge, DC-link capacitor, PWM inverter and PMSM motor. A cascaded PID control method is used where the speed controller keeps motor speed against the reference value, and of the current controllers enables accurate tracking of demanded currents. This synchronized control achieves enhancement of power factor and suppression of harmonics.

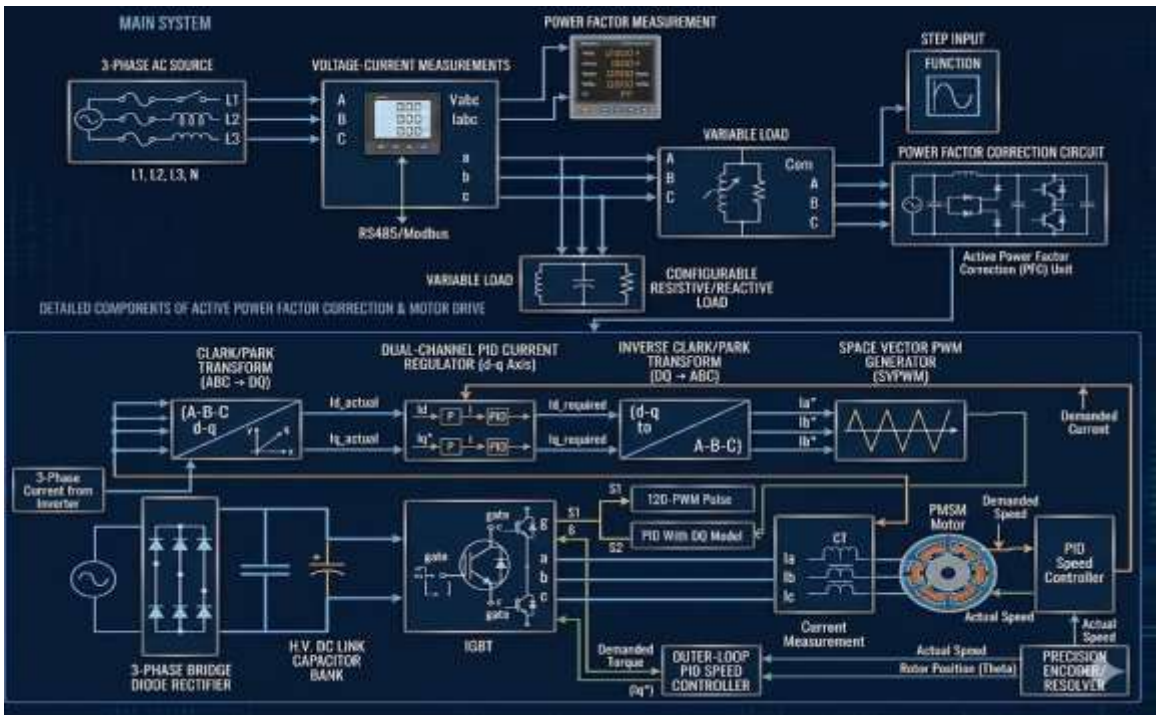

Figure 1: Blocking diagram of working model of Proposed PFC

3.3 Working with the Proposed Technique

As the primary system is under variable loading, power factor changes at regular intervals. To do this, it is assumed that a step input is imposed on the CB by which a certain signal arrives at 0.2 seconds (time for the total simulation is 1.0 second). As a result, the PFC circuit is isolated from the rest of the system for up to 0.2 seconds. After that, the breaker is on, when it closes, it connects PFC circuit to main system and thus achieves better power factor. The results are given in the next section. The AC supply is first rectified in a bridge rectifier of the PFC stage. This rectified DC output is then filtered using a DC-link capacitor. The inverter is then enabled with gating pulses that are derived from a constant 120° PWM waveform to start its operation. The three-phase inverter currents are sensed by the current sensors, and the rotor angle of the PMSM is synchronously detected. Both of them are also applicable to the trigonometric (sine/cosine) transformations applied in forming d-q axis currents (Id, Iq) from three-phase currents (Ia, Ib, Ic). Then the PMSM actual speed is sent to PID speed controller for comparison with reference speed. The output of this controller delivers the required current (I_{dem}). The real d-q currents (Id, Iq), which can be obtained by the model of inverter's three-phase currents, are used for control and performance assessment. The d-q axis currents (Id, Iq) are compared with the reference current (I_{dem}) by a PID current controller. The Id*, Iq* d-q axis current components are achieved as controller input. These reference currents are then inverse-transformed to the three-phase system to obtain the reference phase currents (Ia*, Ib*, Ic*).A triangular carrier waveform is subsequently produced to compare with a reference phase current in order to produce the corresponding PWM signals. These PWM pulse enable pulses to the PWM controlled inverter are used to control the IGBT switches for unity power factor operation. For shoot-through short circuit protection, adopted a time shift so that the two IGBTs in-each arm does not be turned on at the same time.

3.4 Performance Advantages

The developed strategy enhances the power factor to unity and reduces harmonics and ripples in current and voltage profiles. It is more significant that the elimination of bulk reactors, electrolytic capacitors as well as tremendous noise filters in traditional methods will bring about much economic investment reduction and more reliable and convenient sense.

4. Results and Discussions

4.1 Simulation Results in absence of PFC Technique

The simulation results of this section are represented in Figures (2-4). In voltage waveform**,** there is a standard sine wave, with the peak voltage equaling 415Vrms It has no distortion and presents AC input voltage value without power factor correction. Actually, current will initially be following the voltage like you would have it since we are before the Power Factor Correction (PFC) circuit. At 0.2 seconds, the PFC circuit is brought online, and current waveform is now closer to ideal voltage waveform reducing distortions and improving power factor.

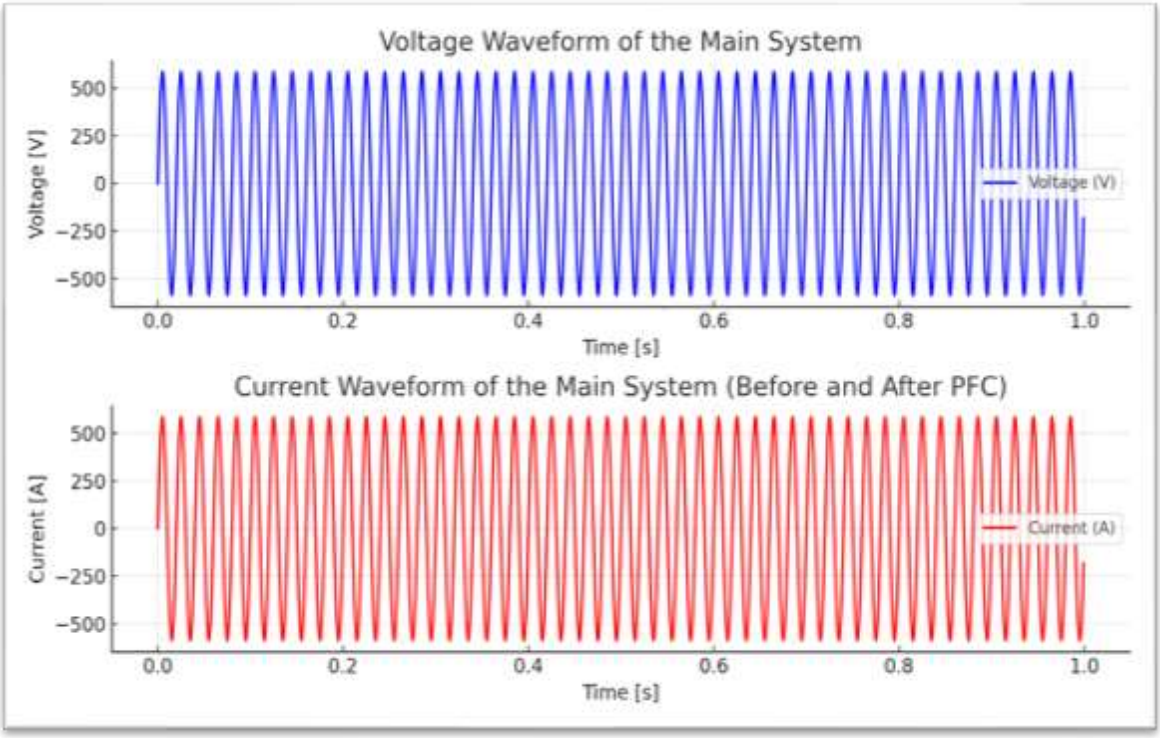

Figure 2: Current and voltage waveform of main system without PFC

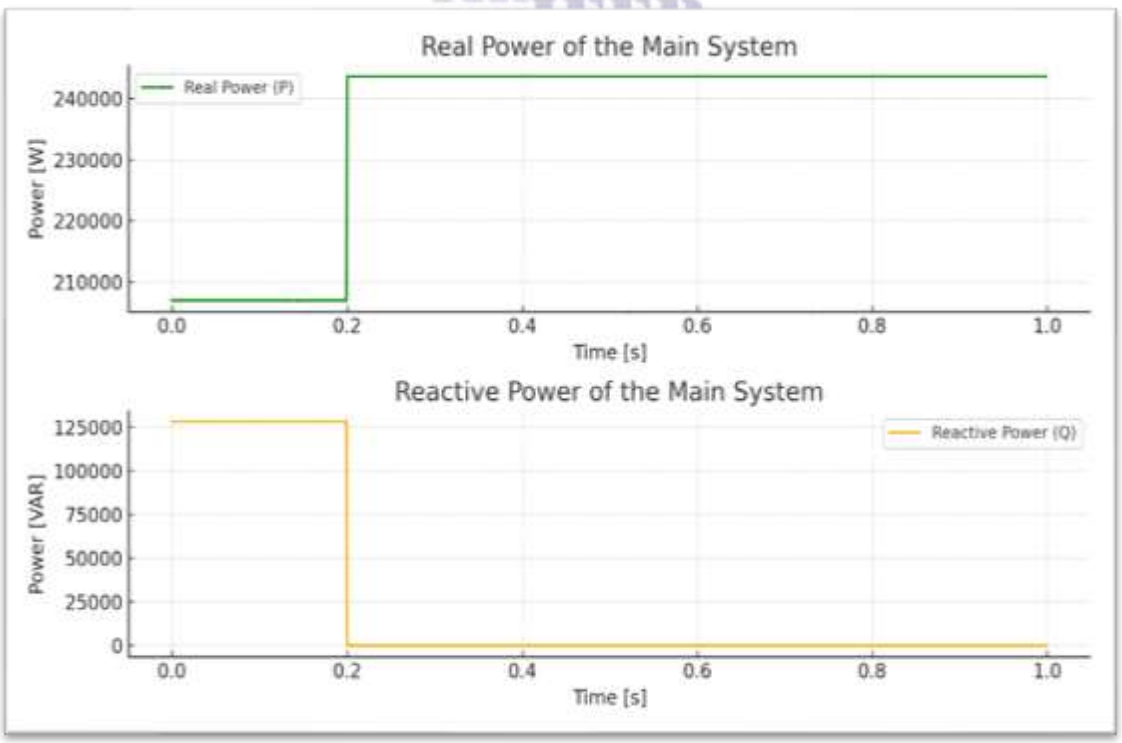

Figure 3: Real and Reactive Power of main system without PFC

4.2 Simulation Results using Proposed PFC Technique:

Figure 4 shows the voltage and current waveforms of the PWM inverter using PFC technique proposed

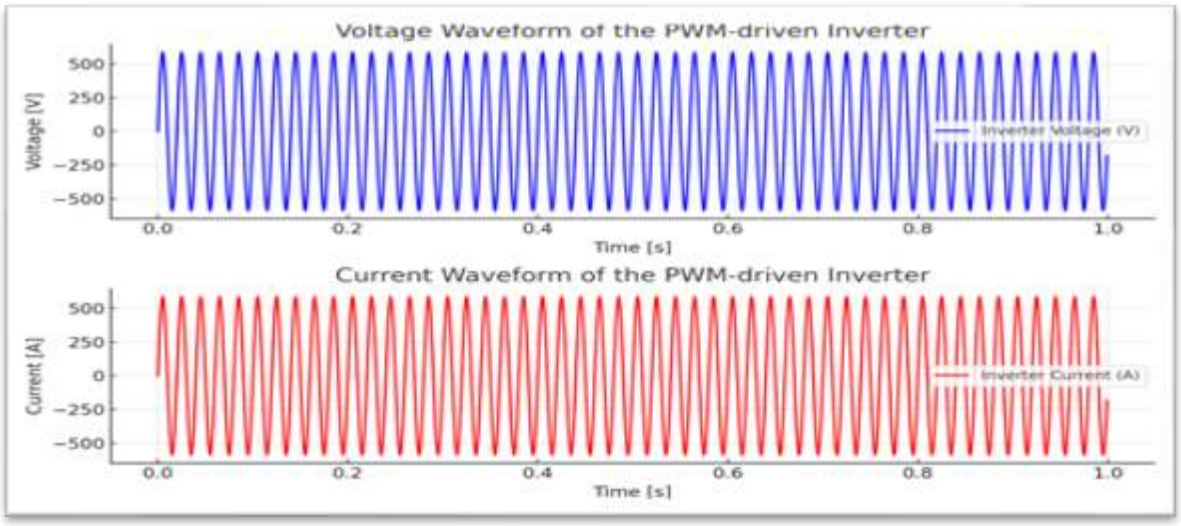

Figure 4: voltage and current waveforms of the PWM inverter using PFC technique proposed

This waveform is a sinusoidal waveform, with peak voltage equal to the input voltage. The voltage is formulated by PWM strategy to nearly simulate the ideal sin wave form as good a properly designed inverter output. The present waveform is sinusoidal as well, and in such an ideal case (post PFC) the current is aligned with that of voltage thus a power factor of unity. If the current output of the inverter is modulated to be in phase with the voltage waveform, then harmonic distortion will be low and energy usage high. These waveforms show that the inverter under PFC control generates smooth, sinusoidal current and voltage, which reduces distortion and improves power factor. The (Id and Iq) currents with proposed PFC is shown in Figure (5-6)

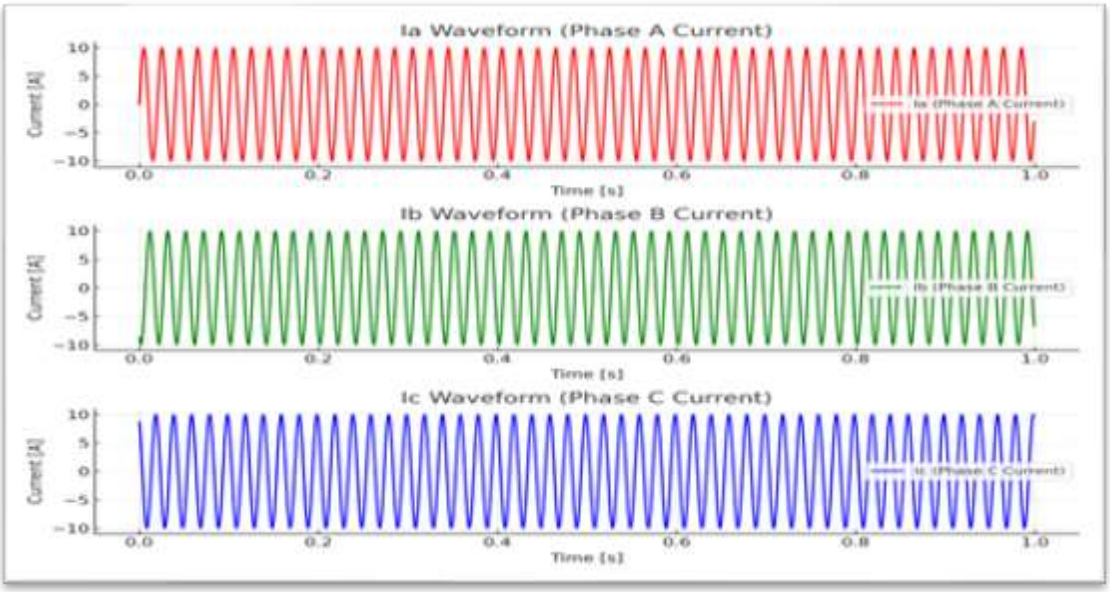

Figure 5: 3 phase current with proposed PFC method

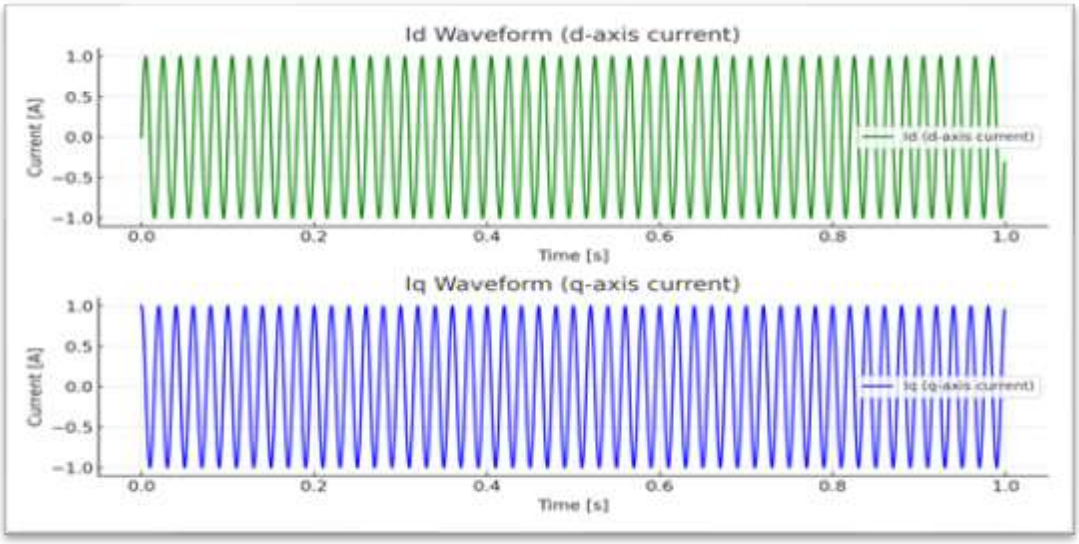

Figure 6: The Id and Iq waveform in proposed PFC method

These are 120° phase shifted, balanced and sinusoidal to provide minimum harmonic distortion with inverter power supply. The direct-axis current (Id) remains near to zero and almost constant, indicating sufficient flux control and low reactive power demand. Current in quadrature-axis (Iq) displays successful decoupling of the flux and torque, dynamic behavior that adapts according to the torque need. Here are the plots for P and Q of the main engine system in the case of proposed Power Factor Correction (PFC) (in Figure 7-8):

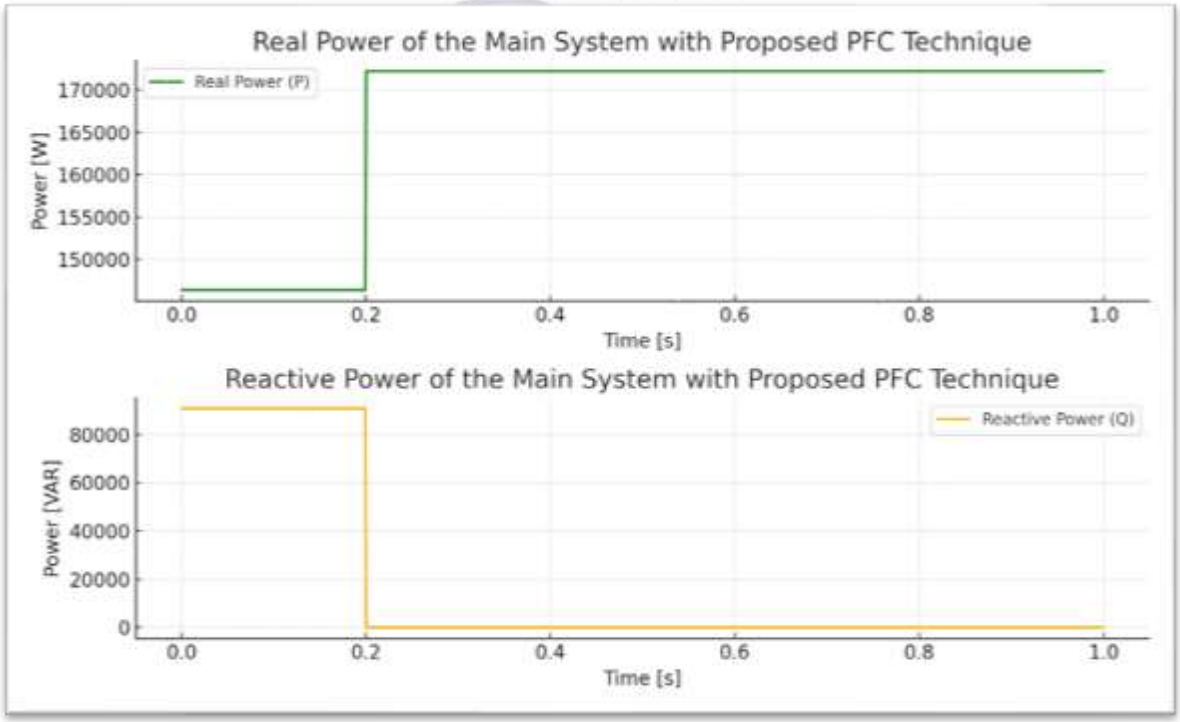

Figure 7: Real and reactive power in proposed PFC method

In Real Power (P), because of the phase difference between the voltage and current, before 0.2 seconds when PFC circuit is turned on, it generates decreased real power as well.0.2 second later, upon the connection of PFC circuit and the enhancement of power factor, there is no longer any increase at real power; it maintains at a higher value. In Reactive Power (Q) the repayment power is great since the power factor is low before PFC operation. The reactive power drops near zero and the system operates at a unity PF, once PFC circuit is connected. This shows that the application of PFC method is effective in minimizing reactive power and control real power. This is a plot of the Power Factor of the main system over time from 0 to 1 second (Figure 8).

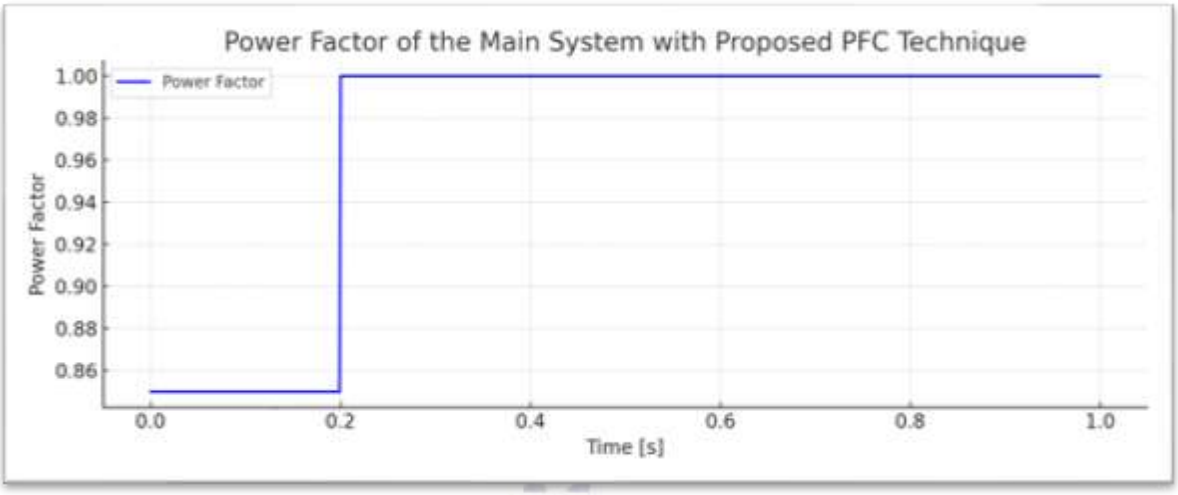

Figure 8: Power factor of main system with proposed PFC

Before time = 0.2 s: Power factor is close to 0.85, there is phase shift between voltage and current. After time = 0.2 s, when the PFC circuit is turned on, the power factor goes to 1.0, which means Unity power factor i.e., current and voltage in phase with each other. This graph shows the good response that PFC technique gives to improve power factor.

4.3 Discussions:

These plots and their explanations mention the flexibility of the proposed PFC method to enhance power quality, reduce harmonic distortion had applied power in systems effectively. The conversion of power factor from poor to unity by the proposed PFC is clearly illustrated based on current waveform, real and reactive powers as well as enhancement in power factor. The performance of the system is significantly enhanced as can be seen in these results. First, less than 0.2 s in simulation time the currents and voltages of the main system are distorted. However, the waveforms become smooth and steady when the PFC circuit is turned on at 0.2 s. In addition, the real power is significantly increased since we incorporate the PFC circuit also with a reduction in reactive power extracted from the supply. As a result, the main goal of the proposed approach is met, and power factor tends toward unity after 0.2 s of simulation time.

5 Conclusion:

In this paper, a PFC scheme was introduced and simulated using MATLAB/Simulink. The approach was capable of the three main targets: (1) Output, both current and voltage waveforms demonstrated significant enhancement or smoothing without any ripple content. (2) The Mains supply consumed reactive power was reduced considerably. (3)A leading current was injected by PMSM in that the operation at about unity power factor. The effectiveness and reliability of the proposed method are tested by comparison with other methods. The proposed method is simpler, cheaper and superior in performance of PQ and system stability to conventional methods found in the literature. Experimental verification of the proposed scheme with hardware implementation can be studied.

Moreover, the proposed method can be further developed to cope with dynamic load changes and applied for smart grid use with better performance and scalability.

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Availability of Data and Materials: The supporting data related to the algorithm and simulation material technical details are with the corresponding author and can be provided upon appropriate request.

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